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09/582,451	11/10/2000	Michael Scott Deiss	RCA88853	3490		
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Robert D. Shedd, Patent Operations THOMSON Licensing LLC P.O. Box 5312 Princeton, NJ 08543-5312			AN, SHAWN S			
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/582,451	DEISS ET AL.	
	Examiner	Art Unit	
	SHAWN AN	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 20 July 2009.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 13-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 13-32 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Response to Amendment

1. As per Applicant's instruction as filed on 7/20/09, claims 1-12 have been canceled, claims 13, 15-18, 20-22, and 24, and claims 25-32 have been newly added.

Response to Remarks

2. Applicant's Remarks as filed on 7/20/09 have been fully considered but they are not persuasive. The Applicant presents main arguments of which the cited prior art references do not disclose or suggest:

- A) a receiver that is adapted to receive both compressed digital signals and analog signals;
- B) specifically, since Fujii does not disclose or suggest a receiver receiving an analog signal, there is no digitized analog signal in the receiver. As such, Fujii does not disclose the delay element in claim 13;
- C) a second input for receiving an analog signal;
- D) a processor processing the analog signal to generate a digitized audio signal and a digitized video signal;
- E) first digital signal processing arrangement decompressing the video component of the packetized data stream, and digital signal processing the decomposed video component and the digitized video signal to generate a video output;
- F) the second digital signal processing arrangement decompressing the audio component of the packetized data stream, and digital signal processing the decompressed audio component and the digitized audio signal to generate an audio output signal; and
- G) a delay selectively delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal (newly amended claim limitation).

However, after careful scrutiny of Applicant's specification, the Examiner disagrees, and maintains the grounds of rejection for the reasons that follow.

Before Examiner's responses, Applicant is reminded that 103 rejections are an obviousness rejection based on combination of references.

In response to argument A), Williams discloses a receiver that is adapted to receive compressed digital signals (Fig. 8; 110). Furthermore, Citta et al clearly teaches/shows a receiver that is adapted to receive an analog signal (RF signal) (Fig. 4, 32; col. 3, lines 39-67). This analog signal is subsequently processed/digitized (via 34) by conventionally well known analog to digital converter (A/D) as shown in Fig. 4, 36.

A combination of William and Citta et al's teachings as directly above would certainly result in the recited "a receiver that is adapted to receive both compressed digital signals and analog signals".

In response to argument B), the Applicant is reminded that Fujii does not have to disclose or suggest a receiver receiving an analog signal, since Citta et al clearly teaches/shows a receiver (Fig. 4, 32) that is adapted to receive an analog signal (RF signal), whereby the analog signal is digitized by the analog to digital converter (A/D) as shown in Fig. 4, 36. (col. 3, lines 39-67).

Furthermore, Fujii et al teaches delaying/adjusting means (Fig. 1, 74) for selectively delaying the processing of the digitized audio signal (from a tuner, 1, receives a channel data comprising encoded QAM, QPSK, or the like) to synchronize an audible audio signal with the displayable video signal, and the delaying means being connected to the second processing means (audio decoder) and the partitioning means (data bus)(col. 1, lines 56-67; col. 7, line 38-col. 8, line 27).

Once again, Applicant is kindly reminded that 103 rejections are an obviousness rejection based on combination of references.

In response to argument C), based on combination of references (Williams in view of Citta et al and Fuji et al), Citta et al's input (the receiver, as discussed above) serves as a second input for receiving an analog signal.

In response to argument D), Citta et al teaches a processor processing the analog signal to generate a digitized audio signal and a digitized video signal (Fig. 4, 36; col. 3, lines 39-67; col. 4, lines 1-5).

In response to argument E), Williams discloses first digital signal processing arrangement (Figs. 7-8, 122) decompressing the video component of the packetized data stream (from 114), and digital signal processing the decompressed video component to generate a video output signal (to T.V., 126). Furthermore, Citta et al teaches a processor processing the analog signal to generate a digitized audio signal and a digitized video signal (Fig. 4, 36; col. 3, lines 39-67; col. 4, lines 1-5).

Therefore, it would have been considered obvious to a person of ordinary skill in the relevant art employing Williams teaching as above to incorporate/combine Citta et al's teaching as above so that first digital signal processing arrangement decompresses the video component of the packetized data stream, and digital signal processes the decomposed video component and Citta et al's digitized video signal to generate a video output.

Once again, Applicant is kindly reminded that 103 rejections are an obviousness rejection based on combination of references.

In response to argument F), Williams discloses second digital signal processing arrangement (Figs. 7-8, 123) for decompressing the audio component of the packetized data stream (from 114), and digital signal processing the decompressed audio component to generate an audio output signal (to T.V., 126; col. 15, lines 54-67; col. 16, lines 1-20). Furthermore, Citta et al teaches a processor processing the analog signal to generate a digitized audio signal and a digitized video signal (Fig. 4, 36; col. 3, lines 39-67; col. 4, lines 1-5).

Therefore, it would have been considered obvious to a person of ordinary skill in the relevant art employing Williams teaching as above to incorporate/combine Citta et al's teaching as above so that the second digital signal processing arrangement decompresses the audio component of the packetized data stream, and digital signal processes the decompressed audio component and Citta et al's digitized audio signal to generate an audio output signal.

Once again, Applicant is kindly reminded that 103 rejections are an obviousness rejection based on combination of references.

In response to argument G) (the newly amended claim limitation), please refer to the following new grounds of rejection incorporating previously cited prior art references as this argument comprises the newly amended claim limitation.

Lastly, in response to Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 13-18, 20-22, and 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (6,134,419) in view of Citta et al (5,602,595) and Fuji et al (5,898,695).

Regarding claims 13, 15-16, 20, and 24, Williams discloses a receiver and a method for processing input signals comprising:

a first input (tuner) (Fig. 8, 110) for receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data (Fig. 1; Fig. 3, 58);

a transport decoder unit (Figs. 7-8, 118, 120) partitioning said packetized data stream to generate a video component and an audio component;

first digital signal processing arrangement (Figs. 7-8, 122) decompressing said video component of said packetized data stream, and digital signal processing said decomposed/decompressed video component to generate a video output signal, and second digital signal processing arrangement (Figs. 7-8, 123) decompressing said

Art Unit: 2621

audio component of said packetized data stream, and digital signal processing said decompressed audio component to generate an audio output signal (col. 15, lines 54-67; col. 16, lines 1-20);

a converting arrangement transposing said video output signal to the displayable video signal (Figs. 7-8, 125) and said audio output signal to the audible output signal (Figs. 7-8, 127).

Williams does not particularly disclose a second input for receiving an analog signal, a processor processing said analog signal to generate a digitized audio signal and a digitized video signal (also recited in the first and second digital signal processing elements), and a delay selectively delaying the processing of the digitized audio signal to synchronize an audible audio signal with a displayable video signal;

However, Citta et al teaches an ATV receiver/sync system comprising an input for receiving an analog signal (Fig. 4, 32), a processor processing said analog signal to generate a digitized audio signal and a digitized video signal in order to provide an improved system for receiving analog and digital data (Fig. 4, 36; col. 3, lines 39-67; col. 4, lines 1-5).

Furthermore, Fujii et al teaches a system comprising a conventional delaying/adjusting means (Fig. 1, 74) for selectively delaying audio signal to synchronize an audible audio signal with the displayable video signal, and the delaying means being connected to the second processing means (audio decoder) and the partitioning means (data bus).

Therefore, it would have been considered obvious to a person of ordinary skill in the relevant art employing a digital receiver as taught by Williams to incorporate/combine Citta et al's teachings as above so that Williams incorporates a second input for receiving an analog signal and a processor processing the analog signal to generate a digitized audio signal and a digitized video signal, and that first digital signal processing arrangement decompresses the video component of the packetized data stream, and digital signal processes the decomposed video component and Citta et al's digitized video signal to generate a video output and the second digital signal processing arrangement decompresses the audio component of the packetized

Art Unit: 2621

data stream, and digital signal processes the decompressed audio component and Citta et al's digitized audio signal to generate an audio output signal in order to provide an improved system for receiving analog and digital data, and to incorporate/combine Fuji et al's adjustable delay means so as to selectively delay Williams' audio output signal, wherein the delay includes the partitioning means, in order to synchronize an audible audio signal with a displayable video signal.

Regarding claim 14, Fujii et al discloses providing an adjustable memory device (Fig. 1, RAM).

Regarding claims 17-18, Williams discloses a processing element (127) digital signal processing the decompressed audio component. Citta et al teaches a processor digital signal processing the analog signal to generate a digitized audio signal in order to provide an improved system for receiving analog and digital data (Fig. 4, 36; col. 3, lines 39-67; col. 4, lines 1-5).

Furthermore, subsequent/secondary audio processing such as Six Channel Dolby Digital Surround Sound Processor was well known at the time the invention was made.

Therefore, it would have been considered obvious to a person of ordinary skill in the relevant art employing Williams' teaching as above to incorporate/combine Citta et al's teaching as above so that the processing element digital signal processes the decompressed audio component, and Citta et al's digitized audio signal in order to provide an improved system for receiving analog and digital data.

Regarding claims 21-22, 25-30, and 32, as Fujii et al teaches a conventional delaying means (Fig. 1, 74) for selectively delaying audio signal to synchronize an audible audio signal with the displayable video signal, it would have been considered simply obvious to perform delaying before or after the step of digital signal processing Citta et al's digitized audio signal has been completed as a matter of a simple design choice as desired by an operator/designer.

Regarding claim 31, Williams discloses a converting element (125) digital signal processing the decompressed video component. Citta et al teaches a processor digital signal processing the analog signal to generate a digitized video signal in order to

provide an improved system for receiving analog and digital data (Fig. 4, 36; col. 3, lines 39-67; col. 4, lines 1-5).

Therefore, it would have been considered obvious to a person of ordinary skill in the relevant art employing Williams' teaching as above to incorporate/combine Citta et al's teaching as above so that the converting element digital signal processes the decompressed video component, and Citta et al's digitized video signal in order to provide an improved system for receiving analog and digital data.

5. Claims 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams, Citta et al, and Fuji et al as applied to claims 12 and 20 above, respectively, and further in view of Dean (5,963,261).

Regarding claims 19 and 23, Williams does not particularly disclose a converter for converting the digitized interlace video format into a digitized video signal having a progressive scan format.

However, Dean teaches a conventional converter for converting the interlace video format into a video signal having a progressive scan format (Fig. 1), such as to be used for a digital receiver for providing high quality pictures (abs.; col. 3, lines 1-3 and lines 33-50).

Therefore, it would have been considered obvious to a person of ordinary skill in the relevant art employing a digital receiver as taught by Williams' to incorporate/combine Dean's teaching as above so that the converter converts the digitized interlace video format into the digitized video signal having a progressive scan format in order to provide high quality pictures.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to *Shawn An* whose telephone number is 571-272-7324.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418.

8. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SHAWN AN/

Primary Examiner, Art Unit 2621

12/22/09

Application/Control Number: 09/582,451
Art Unit: 2621

Page 10